Preliminary Design and Comparative Analysis Between Different DT Sigma-Delta Modulators

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***Abstract*—Sigma-Delta analog-to-digital converters (ADCs) are known for providing high resolutions when compared to other ADC architectures. They are composed of a sigma-delta modulator and a digital decimation filter. This work focuses is in the high-level design of discrete-time sigma-delta modulators (DT-SDMs) whereas the design and implementation of first and second-order modulators are analyzed using Matlab. A complete performance analysis of each modulator is described using the cascade of integrators in feedback (CIFB) structure. It is worth mentioning that our study has a focus on medium bandwidth (BW) applications, as such audio applications. Besides, we target low-voltage operations. This work is at an early stage, thus only first and second-order modulators are investigated. This work considers a BW of 24 kHz, a sampling frequency of 6.144 MHz, and oversampling (OSR) of 128.**

***Index Terms*—sigma-delta modulators, sigma-delta ADC, DT-SDM CIFB structure.**

I. Introduction

Sigma-delta analog-to-digital converters (ADCs) have been widely used in systems that require high resolution for information processing. Basically, sigma-delta ADCs are composed of a sigma-delta modulator (SDM) and a decimation filter. The SDM is composed of a quantizer and integrators, with the number of integrators determining the order of the modulator [1], [2].

SDMs can be implemented in discrete time (DT) or continuous time (CT). In general, the CT-SDM design has greater complexity compared to the SDM-DT [3]. However, they are more energy efficient and can achieve higher bandwidths (BW). On the other hand, in these modulators, the loop filter coefficients depend on the sampling frequency, making them limited to operating at only one fixed frequency. As for DT-SDM, based on switched capacitors, the sampling frequency can be changed without changing the loop filter coefficients. With this, the BW of the signal and the sampling frequency can be changed directly.

This work presents a comparative analysis, design, and implementation of first and second-order DT-SDMs. This study focuses on applications that require audio bandwidth and low supply voltage. From this, we consider a BW of 24 kHz, a sampling frequency of 6.144 MHz, and an oversampling ratio (OSR) of 128. The results were extracted exclusively by simulations performed in Matlab/Simulink® with the aid of DSToolbox by Richard Schreier [3].

This article is organized as follows: in Section II we present high-level metrics for the Sigma-Delta modulator design. In Section III we present and discuss the DT-SDM design results. Finally, the conclusions and final considerations are addressed in Section IV.

II. Sigma-Delta Modulator Performance Parameters

This section presents the main metrics to evaluate SDMs. It is important to evaluate the performance of the developed modulators as well as their operating range.

A way to characterize a SDM is by conducting a detailed analysis of its performance parameters, including dynamic range (DR), effective number of bits (ENOB), and signal-to-noise-and-distortion ratio (SNDR). The dynamic range is determined by the signal amplitude related to full-scale when the SNDR of the modulator is zero. Its value is lower but close to the peak SNDR. Additionally, the SNDR represents the relationship between the power of the input signal and the total noise of the circuit during the quantization process, including harmonic components [4]. Lastly, ENOB is calculated based on the SNDR [5] and is given by

$$ENOB \approx \frac{SNDR - 1.76}{6.02}. \tag{1}$$

When the order of the SDM increases, it results in a better performance of the DR, on the other hand, the system becomes more susceptible to instability for orders greater than four. Fig. 1 shows the estimated DR as a function of the oversampling rate for L-orders from SDMs.

III. High-Level Design and Simulation

The system-level design parameters of the modulator blocks are the main point of this section. Ideal parameters and modulator coefficients are obtained through the toolbox functions and these values are optimal for providing maximum signal-to-noise ratio (SNR) [6]. A first and second-order DT-SDM are designed in this section for comparison between their characteristics.

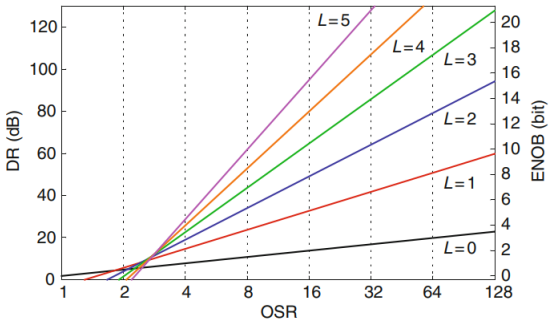

Fig. 1: Ideal DR vs OSR for an L-order SDM.

TABLE I: DT-SDM design parameters

Parameters	Value
Supply Voltage	1.2V
Loop Filter Order	1 and 2
Sample frequency (Fs)	6.144MHz
Bandwidth (BW)	24 kHz
Quantization Levels (Nlev)	2
Oversampling Ratio (OSR)	128

Fig. 2 represents a block diagram for a first-order DT-SDM using a cascade of integrators in feedback (CIFB). The modulators were initially designed by modeling the noise-transfer-function (NTF) of the SDMs. These parameters depend on the modulator's order, sampling frequency, quantization levels (Nlev), and oversampling ratio. Table I specifies the design parameter values for the explored modulators.

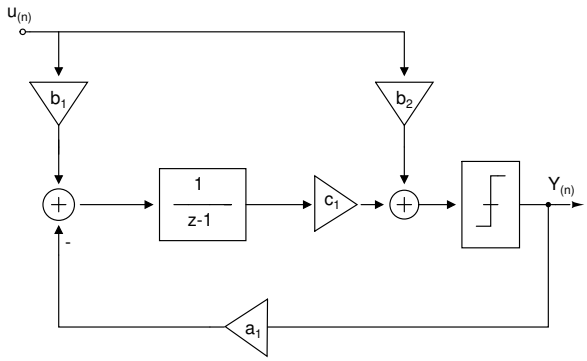

Fig. 2: First-order DT-SDM with CIFB structure.

The first and second-order NTFs are given by equations 2 and 3, respectively. The pole-zero diagram and frequency response of both NTFs are shown in Fig. 3 and 4. For the first-order modulator, the NTF gain is -33.43 dB while the second-order modulator has a NTF gain of -61.5 dB.

$$NTF_{MOD1} = \frac{z-1}{z-0.3333} \tag{2}$$

$$NTF_{MOD2} = \frac{(z-1)^2}{z^2-1.225z+0.4415} \tag{3}$$

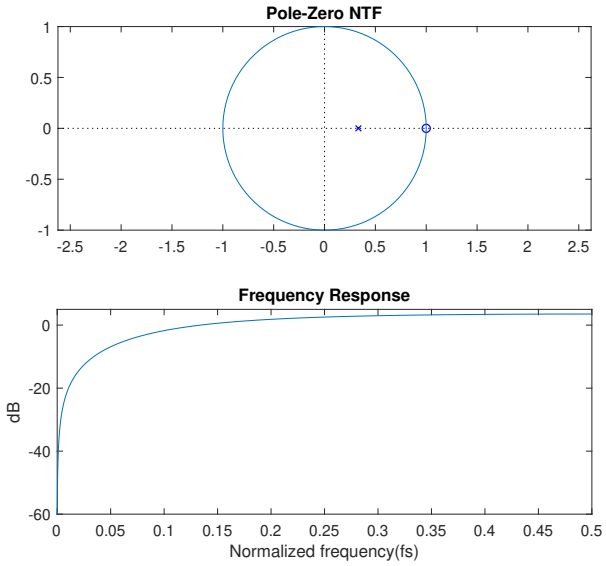

Fig. 3: NTF response for the first-order modulator.

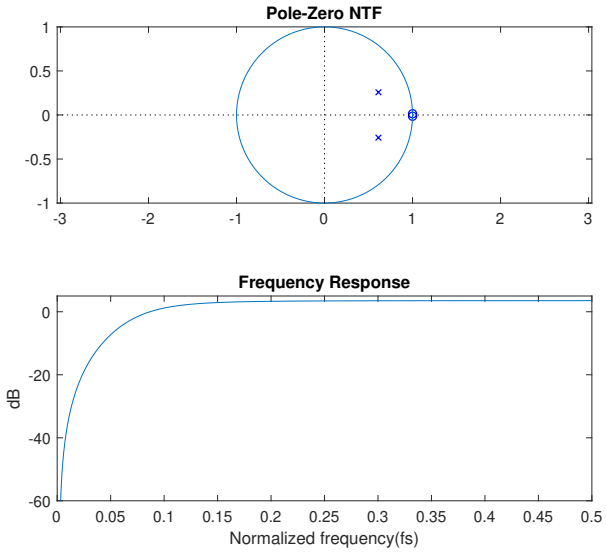

Fig. 4: NTF response for the second-order modulator.

The amplitude of the input signal was chosen as half of the fullscale voltage and the coherent input frequency was $f_{in} = 1.9688$ kHz. The SNR of the output modulator and expected power spectrum density (PSD) can be observed in Fig. 5 and 6. The response of the modulators represents its relation-signal-to-noise (SNR) of 62.5 dB for the first order and 88.4 dB for the second order.

Another characteristic to be observed about these modulators is the peak SNR, this ratio is the maximum in signal amplitude and the output of the modulator, is determined for the NTF of the modulator and the quantizers levels, these are shown in Fig. 7 for the first order and the Fig. 8 for the second order.

Once the NTF design satisfies the premeditated performance, we can determine the coefficients of the state space

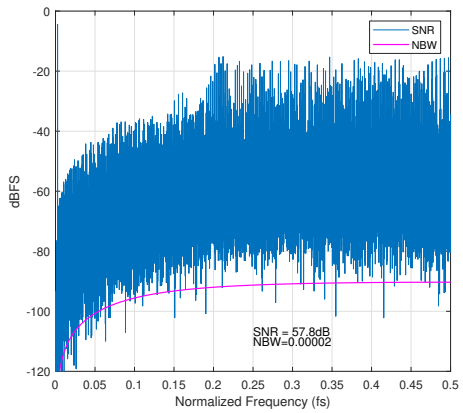

Fig. 5: SNR and expected PSD of the first order modulator.

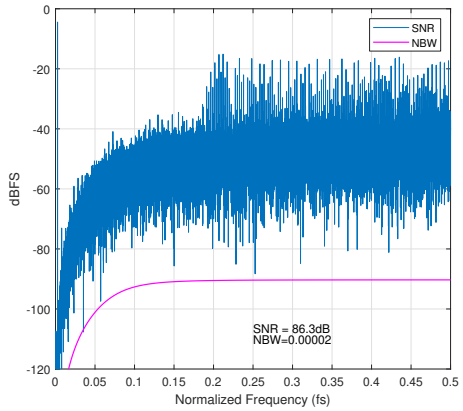

Fig. 6: SNR and expected PSD of the second order modulator.

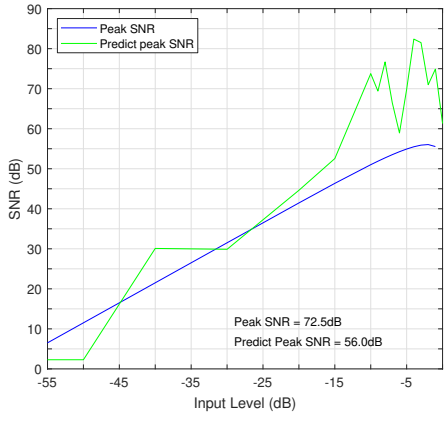

Fig. 7: SNR peak first order modulator

ABCD matrix when we compute a generic loop filter for a specific structure, in this case, we use Cascaded Integrators in Feedback (CIFB) and return the coefficients a, b, c and g. These coefficients returned from the ABCD matrix are for an unspecified state and must be limited by the dynamic range of the modulator. These coefficients are presented in Tables II and III.

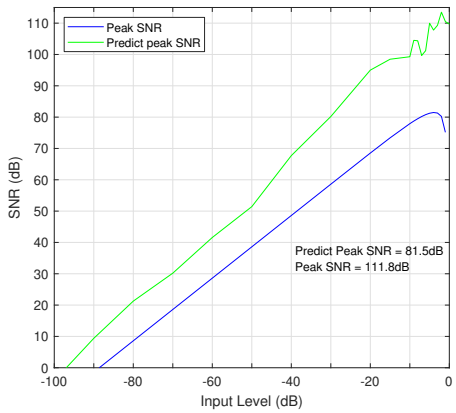

Fig. 8: SNR peak second order modulator

TABLE II: Scaling coefficients of the first-order modulator.

Coef.	Scaling 0.5FS
a1	0.2111
b1	0.2111
b2	1
c1	3.1574
a2, c2	0

A. Simulink Modeling

Previously designed DT-SDMs are implemented in a block diagram in Simulink, where the characteristic topology gain coefficients are employed. These coefficients are the modulator inner loop feedback gains for the CIFB topology and are represented in Fig. 9 and 10.

The output power spectrum density of first- and second-order SDMs are shown in Figs. 11 and 12, respectively. The values of SNR/SNDR and ENOB of both modulators are summarized in Table IV. As expected the second-order modulator presents higher values of SNR/SNDR/ENOB and one extra bit of enob is achieved by using optimized zeros in the noise transfer function (NTF).

TABLE III: Scaling coefficients second-order modulator.

Coef.	Scaling 0.5FS
a1	0.3877
a2	0.0828
b1	0.2162
b2	0.7749
b3	1
c1	0.0569
c2	0.3629
a3, c3	0
g	0.0034

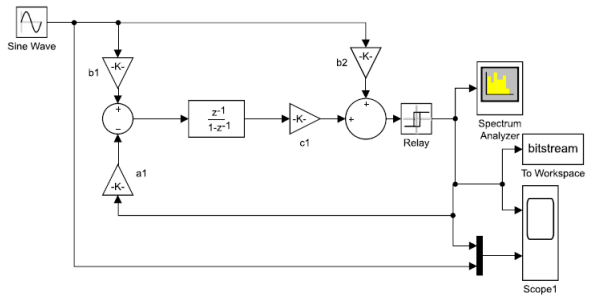

Fig. 9: First Order Modulator at System Level

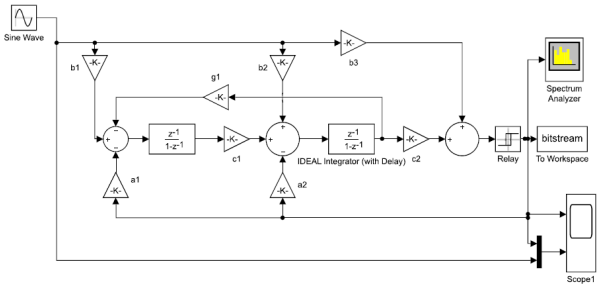

Fig. 10: Second Order Modulator at System Level

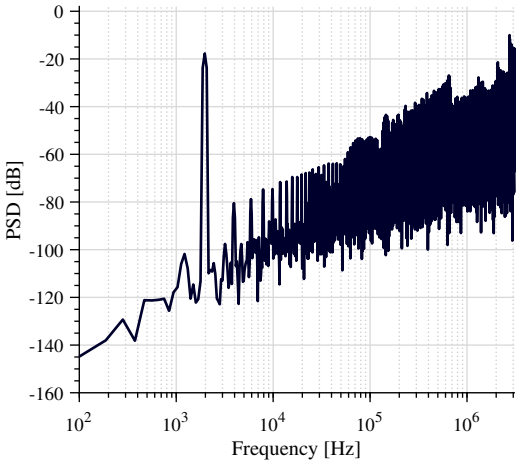

Fig. 11: Power Spectral Density SDM MOD1.

IV. Conclusions

This paper presented the high-level implementation and comparison between first and second-order discrete-time sigma-delta modulators implemented with the CIFB structure. The system-level implementation and all simulation results were extracted exclusively from the Matlab/Simulink®. The obtained values of SNR/SNDR/ENOB for the first and second-order modulators are respectively, 47.76 dB/42.34 dB/6.74 bits and 85.39 dB/84.73 dB/13.78 bits. The main characteristics of these modulators are shown and the data obtained satisfy the expected performance for them. Finally, as future work, implementations of modulators at the level of circuits based on switched capacitors will be carried out. Once this step is completed, we will start building the layout and, later, the prototype of the system using the 65-nm CMOS process.

TABLE IV: Output data Simulink models.

	SNR	SNDR	ENOB
First Order	42.76 dB	42.34 dB	6.74 bits
Second Order	85.39 dB	84.73 dB	13.78 bits

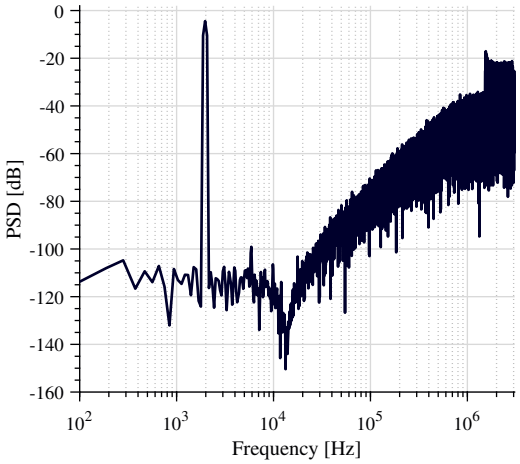

Fig. 12: Power Spectral Density SDM MOD2.

Acknkowlegments

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